IN THE U.S. PATENT AND TRADEMARK OFFICE

#32

Applicant: **Gerard Chauvel, Et al.** TI No.: **15767A**

Serial No.: ~~09~~/08/**890,894** Art Unit: **2186**

Filed: **07/10/1997** Examiner: **Tran, Denise**

For: **Multiple Processor Apparatus Having A Protocol Processor Intended For The Execution Of A Collection of Instructions In A Reduced Number Of Operation** Conf. No.: **5253**

APPEAL BRIEF TRANSMITTAL FORM

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8 (A)

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Elizabeth Austin — Date 12/10/2002

Assistant Commissioner for Patents

Washington, DC 20231

Dear Sir:

Transmitted herewith in triplicate is an Appellant's Brief in the above-identified application.

Charge any additional fees, or credit overpayment to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. An original and two copies of this sheet are enclosed.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	**TIF-15767A**
Gerard Chauvel, et al.	Examiner: **Tran, D.**
Serial No.: **08/890,894**	Art Unit: **2186**
Filed: **07/10/97**	Conf. No.: **5253**

For: **MULTIPLE PROCESSOR APPARATUS HAVING A PROTOCOL PROCESSOR INTENDED FOR THE EXECUTION OF A COLLECTION OF INSTRUCTIONS IN A REDUCED NUMBER OF OPERATIONS**

APPELLANTS' BRIEF

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In support of their appeal of the Final Rejection of claims in the above-referenced application, Appellants respectfully submit herein their Brief and Appendix (attached thereto).

I. REAL PARTY IN INTEREST

Texas Instruments Incorporated is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

Appellants filed a Notice of Appeal on related application 09/606,057 (MULTIPLE PROCESSOR CELLULAR RADIO) on September 18, 2002. Appellants anticipate filing an Appeal Brief in that application shortly.

III. STATUS OF CLAIMS

Claims 6-15, 17, 19, and 34-39 are pending in the application. Claim 19 has been allowed. Final Rejection of Claims 6-15, 17 and 34-39 was made by the Examiner in the Office Action dated June 6, 2002. Claims 6-15, 17 and 34-39 are on appeal. Claims 6-15, 17 and 34-39 are reproduced in the Appendix to Appellants' Brief filed herewith.

IV. STATUS OF AMENDMENTS

Appellants filed an amendment under 37 C.F.R. 1.116 on August 6, 2002, in response to the final rejection of June 6, 2002. In the Advisory Action dated September 4, 2002, the Examiner indicated that for purposes of appeal, the proposed amendment will be entered.

V. SUMMARY OF THE INVENTION

One embodiment of the invention comprises: a first processor (6) for performing scalar processing, said first processor comprising a core (9), a program memory (13) and a local memory (14); a second processor (5) for performing vector processing, said second processor comprising a core (8), a program memory (11) and a local memory (12); a synchronizing circuit (10) for coupling said core of said first processor to said core of said second processor; and a memory circuit (15) for coupling said local memory of said first

processor to said local memory of said second processor (see Figure 5; page 1, lines 7-22; page 5, line 31 - page 6, line 7; page 6, lines 23-26).

Another embodiment of the invention comprises: a first processor (5) comprising a core (8), a program memory (11) and a local memory (12); a second processor (6) comprising a core (9), a program memory (13) and a local memory (14); a synchronizing circuit (10) for coupling said core of said first processor to said core of said second processor; and one and only one common memory (10) coupling said local memory of said first processor to said local memory of said second processor (see Figure 5; page 5, line 31 - page 6, line 7; page 6, lines 23-26).

Still another embodiment of the invention comprises: a main processor (5) comprising a core (8), a program memory (11) and a local memory (12); a protocol processor (6) comprising a core (9), a program memory (13) and a local memory (14); a synchronizing circuit (10) for coupling said core of said main processor to said core of said protocol processor; and one and only one common memory (15) coupling said local memory of said main processor to said local memory of said protocol processor (see Figure 5; page 5, line 31 - page 6, line 7; page 6, lines 23-26).

Yet another embodiment of the invention comprises: a main processor (5) comprising a core (8), a program memory (11) and a local memory (12); a protocol processor (6) comprising a core (9), a program memory (13) and a local memory (14), said protocol processor being suited to execute tasks to which the main processor is not suited; a synchronizing circuit (10) for coupling said core of said main processor to said core of said protocol processor; and a common memory (15) coupling said local memory of said main processor to said local memory of said protocol processor (see Figure 5; page 2, lines 6-15; page 5, line 31 - page 6, line 7; page 6, lines 23-26).

Still yet another embodiment of the invention comprises: a main processor (5) comprising a core (8), a program memory (11) and a local memory (12); a protocol processor (6) comprising a core (9), a program memory (13) and a local memory (14), said

protocol processor being suited to execute tasks to which the main processor is not suited; a synchronizing circuit (10) for coupling said core of said main processor to said core of said protocol processor; and one and only one common memory (15) coupling said local memory of said main processor to said local memory of said protocol processor (see Figure 5; page 2, lines 6-15; page 5, line 31 - page 6, line 7; page 6, lines 23-26).

VI. ISSUES

1) Are Claims 36-39 patentable under 35 U.S.C. 102(b) over Finch et al., U.S. Patent No. 4,783,778?

2) Are Claims 6-7, 9-15, 17 and 36 patentable under 35 U.S.C. 103(a) over Aoyama et al., U.S. Patent No. 4,964,035 in view of Asano et al., U.S. Patent No. 5,237,686?

3) Are Claims 8 and 35 patentable under 35 U.S.C. 103(a) over Aoyama et al., U.S. Patent No. 4,964,035 in view of Asano et al., U.S. Patent No. 5,237,686, further in view of Morris Mano, Computer system architecture, 1982, pages 264 and 282-283?

4) Are Claims 34-35 and 37-39 patentable under 35 U.S.C. 103(a) over Aoyama et al., U.S. Patent No. 4,964,035 in view of Asano et al., U.S. Patent No. 5,237,686, further in view of applicants admitted prior art, Background of the invention, the instant specification page 1 line 6 to page 2, line 11?

5) Are Claims 34-35 and 37-39 patentable under 35 U.S.C. 103(a) over Aoyama et al., U.S. Patent No. 4,964,035 in view of Asano et al., U.S. Patent No. 5,237,686, further in view of Finch et al., U.S. Patent No. 4,783,778?

VII. GROUPING OF CLAIMS

Claims 6-15, 17 and 34-39 stand separately.

VIII. ARGUMENT

The Rejection

Claims 36-39 stand rejected under 35 U.S.C. 102(b) as being anticipated by Finch et al., US Patent No. 4,783,778, hereinafter Finch.

As per claims 36-39, Finch teaches the invention as claimed, an apparatus comprising: a first processor or a protocol processor (e.g., fig. 1, b processor) where the first processor being suited to execute tasks to which a main processor is not suited (e.g., B processor performing x.25 protocol processing, col. 14, line 48 and a processor controlling mini packet protocol, Netlink protocols, initialization, col. 8, line 31 and et seq.), comprising a core (e.g., fig. 1, el. 65sc102), a program memory (e.g., col. 14, line 22 and et seq. or col. 8, line 38 and et seq.), and a local memory (e.g., fig. 1, buffer of B processor or col. 6, line 62 and et seq.); a second processor or the main processor (e.g., fig. 1, A processor; and col.8, line 36 and et seq.), where the second processor, of a design other than the first processor (e.g., fig. 1, A processor comprising: ROM and minipacket receiver/transmitter (MPRT), of a design other than B processor having protocol serial controller (MPSC) and baud rate generation circuit), comprising a core (e.g., fig. 1, el. 65sc102), a program memory (e.g., fig.1, ROM), and a local memory (e.g., fig. 1, RAM of A processor); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig. 1, col. 8, line 55 and et seq., or fig. 1, el. Common memory interface and control); and one and only one common memory coupling the local memory of the first processor to the local memory of the second processor (e.g., fig. 1, common memory).

Claims 6-7, 9-15 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4,964,035, (hereinafter Aoyama) in view of Asano et al., U.S. Patent No. 5,237,686 (hereinafter Asano).

As per claims 6 and 36, Aoyama teaches the invention substantially as claimed, comprising: a first processor for performing scalar processing (e.g., fig. 1, el. 600), comprising a core (e.g., fig.1, el. 601); a second processor for performing vector processing, of a design other than the first processor (e.g., fig. 1, el. 500, vector processor), comprising a core (e.g., fig. 1, els. 501); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig. 1, els 810 or 800a, cols. 5-6); and a common memory circuit for coupling the first processor to the second processor (e.g., fig. 1, el. 800). Even though Aoyama teaches the use of a local buffer, and a program register of a scalar processor (e.g., fig. 1, els. 601 and 602; and col. 5, lines 47 et seq.); and a local register and program register of a vector processor (e.g., fig. 1, el. 502; and col. 8, lines 4 et seq.). Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

As per claim 7, Aoyama shows the use of the second processor being a main processor (e.g., col. 4, line 63 and et seq.).

As per claim 9, Aoyama does not specifically show the second processor as a DSP. Asano (e.g., col. 1, line 9 and et seq.) has been cited as merely one example, to show the concept and advantages of providing DSP to perform signal processing are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Asano into the vector processing system of Aoyama because it would provide signal processing capability to suit a special purpose application, thereby increase system functionality.

As per claims 10-13, Aoyama does not specifically show the local memories as RAM; the program memory as a ROM. Asano (e.g., figs. 1-2, els 22, 17; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of having a local memory as RAM and a program memory for each processor are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Asano into the system of Aoyama because it would allow a storage location to be read and written in any order by having local RAM and increase processing speed of each processor by having local RAM memories and program memories, thereby increasing the processing efficiency for each processor. Aoyama and Asano do not explicitly show a program memory as a ROM. Official Notice is taken that both the concept and advantages of providing; a program memory as ROM are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include ROMs into the system of Aoyama because it would allow a storage system not to loose data when power is removed from it.

As per claim 14, 15, and 17, Aoyama teaches the memory circuit coupling between the first and second processors being physically separate from the first and second processors (e.g., fig.1, el. 800); the memory circuit being DPRAM memory (e.g., col. 10); and the synchronizing circuit ensure that only one of the processors utilized the memory circuit at any one time (e.g., cols. 5-6). Aoyama does not explicitly show the use each of the processor comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local

memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

Claims 8 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4,964,035, (herein after Aoyama), in view of Asano et al., U.S. Patent No. 5,237,686 (hereinafter Asano), further in view of Morris Mano, Computer System architecture, 1982, pages 264 and 282-283, (hereinafter Mano).

As per claim 8, Aoyama does not specifically show the scalar processor as a microprocessor. Mano, page 264, line 8 and et seq., is cited merely as an example to show both the concept and advantages of providing a processor into a microprocessor are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a processor into a microprocessor to Aoyama because it would provide for a reduction in space and signal lines between functional elements, leading to an increase in processing performance.

As per claim 35, Aoyama teaches the vector processor and matrix computations (e.g., fig. 1., els 500 and 600 and cols. 2, line 5 and et seq.); and the scalar processor (e.g., fig., els 500 and 600 and cols. 2, lines 5 and et seq.) but does not explicitly show the use of vector processing including signal processing tasks generally carrying out by a DSP and matrix computation performed by an array processor. Asano (e.g., col. 1, line 9 and et seq.)

has been cited as merely one example, to show the concept and advantages of providing DSP to perform signal processing are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the vector processing system of Aoyama because it would provide signal processing capability to suit a special purpose application, thereby increase system functionality. Mano, e.g., page 282 line 36 and et seq., has been cited as an example to show that both the concept and advantages of providing vector processing including the use of array processor for performing matrix computations are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include an array processor into Aoyama because it would allow parallel computations on large arrays to be performed, thereby, increasing system computation power.

Claims 34-35 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4,964,035, (herein after Aoyama) in view of Asano et al., U.S. Patent No. 5,237,686 (hereinafter Asano), further in view of applicants admitted prior art, Background of the invention, the instant specification page 1 line 6 to page 2, line 11 (hereinafter AAPA).

As per claims 34-35, Aoyama teaches the vector processor and matrix computations (e.g., fig. 1., els 500 and 600 and cols. 2, line 5 and et seq.); and the scalar processor (e.g., fig., els 500 and 600 and cols. 2, lines 5 and et seq.) but does not explicitly show the use of scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and tasks which are generally carry out by hard-wired logic which are the protocol processing, and vector processing including signal processing tasks generally carrying out by a DSP and the use of array processor type. Asano (e.g., col. 1, line 9 and et seq.) has been cited as merely one example, to show that both the concept and advantages of providing DSP to perform signal processing are well known and expected in the art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the vector processing of

Aoyama because it would provide signal processing capability to suit a special purpose application, thereby increase system functionality. Also, AAPA, the instant specification, e.g., page 1 line 6 to page 2, line 11, has been cited as an example to show that both the concept and advantages of providing scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and tasks which are generally carry out by hard-wired logic which are the protocol processing or a protocol processor; and vector processing including the use of array processor type are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing and an array processor performing array computations into Aoyama because it would allow protocol processing to be performed and parallel computations on large arrays to be performed, thereby, increasing system computation power and functionality.

As per claims 37-39, Aoyama teaches the invention substantially as claimed, comprising: a first processor for performing scalar processing of a design other than a main processor (e.g., fig. 1, el. 600), comprising a core (e.g., fig.1, el. 601) where the first processor being suited to execute tasks to which a main processor is not suited; a second processor or the main processor (e.g., col. 4, line 63 and et seq.), for performing vector processing (e.g., fig. 1, el. 500, vector processor), comprising a core (e.g., fig. 1, els. 501); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig. 1, els 810 or 800a, cols. 5-6); and a common memory coupling the first processor to the second processor (e.g., fig. 1, el. 800). Even though Aoyama teaches the use of a local buffer, and a program register of a scalar processor (e.g., fig.1, els. 601 and 602; and col. 5, lines 47 et seq.); and a local register and program register of a vector processor (e.g., fig. 1, el. 502; and col. 8, lines 4 et seq.). Aoyama does not explicitly show the use of each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a

first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor. Aoyama and Asano do not explicitly show the use of the first processor being a protocol processor. AAPA, the instant specification page 1 line 6 to page 2, line 11, has been cited as an example to show that both the concept and advantages of providing protocol processing are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing because it would allow protocol processing to be performed; thereby, increasing system functionality.

Claims 34 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4,964,035, (herein after Aoyama) in view of Asano et al., U.S. Patent No. 5,237,686 (hereinafter Asano), further in view of Finch et al., U.S. Patent No. 4,783,778, (hereinafter Finch).

As per claim 34, Aoyama teaches the vector processor and matrix computations (e.g., fig. 1., els 500 and 600 and cols. 2, line 5 and et seq.); and the scalar processor (e.g., fig., els 500 and 600 and cols. 2, lines 5 and et seq.) but does not explicitly show the use of scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and tasks which are generally carry out by hard-wired logic which are the protocol processing. Finch, e.g., col. 8, line 42 and et seq., has been cited as an example to show that both the concept and advantages of providing a protocol processor are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama

because it would allow protocol processing to be performed, thereby, increasing system computation functionality.

As per claims 37-39, Aoyama teaches the invention substantially as claimed, comprising: a first processor (e.g., fig.1, el. 600) for performing scalar processing of a design other than a main processor or of a design which enables the processor to execute tasks, where the first processor being suited to execute tasks to which the main processor is not suited; comprising a core (e.g., fig.1, el. 601); a second processor or the main processor (e.g., col. 4, line 63 and et seq.), for performing vector processing (e.g., fig. 1, el. 500, vector processor), comprising a core (e.g., fig. 1, els. 501); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig. 1, els 810 or 800a, cols. 5-6); and a common memory coupling the first processor to the second processor (e.g., fig. 1, el. 800). Even though Aoyama teaches the use of a local buffer, and a program register of a scalar processor (e.g., fig.1, els. 601 and 602; and col. 5, lines 47 et seq.); and a local register and program register of a vector processor (e.g., fig. 1, el. 502; and col. 8, lines 4 et seq.). Aoyama does not explicitly show the use of each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor. Aoyama and Asano do not explicitly show the use of the first processor being a protocol processor. Finch, e.g., col. 8, line 42 and et seq., has

been cited as an example to show that both the concept and advantages of providing a protocol processor performs protocol processing are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed; thereby, increasing system functionality.

APPELLANT'S ARGUMENT

1) Claims 36-39 are patentable under 35 U.S.C. 102(b) over Finch et al, US Patent No. 4,783,778, as set forth below.

Since Claims 36-39 have been rejected under 35 U.S.C. § 102(b), in order that the rejection of Claim 36-39 be sustainable, it is fundamental that "each and every element as set forth in the claims be found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court stated, "The identical invention must be shown in as complete detail as is contained in the ... claim". As set forth below, each and every element of Claims 36-39 are not set forth, either expressly or inherently described, in the Finch reference.

Appellants further respectfully point out that, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 36, as amended, requires and positively recites, an apparatus, comprising: "a first processor comprising a core, a program memory and a local memory", "**a second processor, of a design other than said first processor**, comprising a core, **a program memory** and a local memory", "a synchronizing circuit for coupling said first processor to said second processor" and "one and only one common memory coupling said first processor to said second processor".

Independent Claim 37, as amended, requires and positively recites, an apparatus, comprising: "a main processor comprising a core, a program memory and a local memory", "**a protocol processor, of a design other than said main processor**, comprising a core, **a program memory** and a local memory", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor."

Independent Claim 38, as amended, requires and positively recites, an apparatus, comprising: "a main processor comprising a core, a program memory and a local memory", "**a protocol processor** comprising a core, **a program memory** and a local memory, said protocol processor being of a design which enables said protocol processor to execute tasks to which the main processor is not suited", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "a common memory coupling said local memory of said main processor to said local memory of said protocol processor".

Independent Claim 39, as amended, requires and positively recites, an apparatus, comprising: "a main processor comprising a core, a program memory and a local memory", "a **protocol processor** comprising a core, **a program memory** and a local memory, said protocol processor being of a design which enables said protocol processor to execute tasks to which the main processor is not suited", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor".

In contrast, Finch's "B" processor, does not have a "**program memory**", as required by Claims 36-39. FIG. 1 clearly shows that there is no "program memory" in the "B" processor. Finch further teaches that, "The netlink processor ("A" processor (col. 13, line 23)) starts and stops the Facilities Processor ("B" processor). Even though the Facilities Processor ("B" processor) utilizes 64K of the 80K of parity protected memory provided by

the SPM, of the 64K, 43.5K is allocated to common memory which is accessible to both the "A" and "B" processors, while 20K is accessible to the "B" processor only (col. 16, lines 11-16). None of this memory, however, is within the "B" processor. As a result, Finch fails to teach or suggest, "**a second processor, of a design other than said first processor**, comprising a core, **a program memory** and a local memory", as required by Claim 36, or "**a protocol processor, of a design other than said main processor**, comprising a core, **a program memory** and a local memory", as required by Claim 37, or "**a protocol processor** comprising a core, **a program memory** and a local memory, said protocol processor being of a design which enables said protocol processor to execute tasks to which the main processor is not suited", as required by Claim 38, or "a **protocol processor** comprising a core, **a program memory** and a local memory, said protocol processor being of a design which enables said protocol processor to execute tasks to which the main processor is not suited", as required by Claim 39. Accordingly, the 35 U.S.C. 102(b) of Claims 36-39 as being anticipated by Finch et al, is overcome.

2) Claims 6-7, 9-15, 17 and 36 are patentable under 35 U.S.C. 103(a) over Aoyama et al., U.S. Patent No. 4,964,035 in view of Asano et al., U.S. Patent No. 5,237,686, as set forth below.

Independent Claim 6 requires and positively recites, "a first processor for performing scalar processing, said first processor comprising a core, **a program memory and a local memory**", "a second processor for performing vector processing, said second processor comprising a core, **a program memory and a local memory**", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "a memory circuit **for coupling said local memory of said first processor to said local memory of said second processor**".

Independent Claim 36 requires and positive recites, "a first processor comprising a core, **a program memory and a local memory**", "a second processor, **of a design other than said first processor**, comprising a core, **a program memory and a local memory**",

"a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "**one and only one common memory coupling said local memory of said first processor to said local memory of said second processor**".

The Examiner admits that Aoyama "does not show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor" (Office Action dated June 6, 2002, page 3, line 18 – page 4, line 1). The Examiner relies upon Asano as "teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory" (Office Action dated June 6, 2002, page 4, lines 1-4).

Applicants respectfully traverse the Examiner's interpretation of Asano and point out that Asano's processor DMM1-DMMk (11a-11k) are ALL digital signal processors (Figs. 1 & 2; Col. 9, lines 46-53) which are used exclusively for video signal processing (col. 5, lines 50-55; col. 6. lines 57- col. 8. line 21). Accordingly, since each unit processor DMM1-DMMk is in charge of processing image signals for a plurality of sectional frames which are not contiguous but separated from each other, and all the unit processor simultaneously begin processing in synchronism with the state of a new picture frame, each of processors DMM1-DMMk appear to perform "vector" processing, and not "scalar" processing. Accordingly, it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Asano similarly fails to teach or suggest a "synchronizing circuit for coupling said core of said first processor to said core of said second processor", as required by Claims 6 and 36. Appellants specifically asked the Examiner to identify such circuit in Asano, but the Examiner failed to do so. This is yet another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the

teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Asano further fails to teach or suggest, "one and only one common memory coupling the local memory of the first processor to the local memory of the second processor", as required by Claim 36, since Asano clearly discloses "multiple" common memories 10a-10n coupling processors DMM1-DMMk (Figs. 1 & 2). This is yet still another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing. Accordingly, the 35 U.S.C. 103 rejection of Claims 6 and 36 over a combination of Aoyama and Asano is overcome.

Response to Examiner's rebuttal (10) (Office Action dated June 6, 2002, page 14, line 4 – page 15, line 8). Appellants respectfully traverses the Examiner determination. More particularly, the Examiner never addresses the distinction between Aoyama (which discloses one vector processor and one protocol processor) and Asano, which discloses two vector processors. The Examiner had previously argued that the teachings of one can be lumped into the teaching of the other. Now, the Examiner states that "he would apply the teaching of Asano as set forth by the Examiner to modify the Aoyama but would not physically combine the two system together (Office Action dated June 6, 2002). Obviously, the reason why the Examiner will not combine the two references is because they CANNOT be combined! The Examiner provides no teaching from the prior art that indicates that the teaching of Asano can be combined with Aoyama in order to modify Aoyama, with any hope of success in arriving at a modified apparatus that obviates the present invention. Where is the evidence that such a combination is 1) desirable, or 2) possible? The Examiner's determination is supposition not supported by fact.

Response to Examiner's rebuttal (11) (Office Action dated June 6, 2002, page 15, lines 9-15). Appellants respectfully traverse the Examiner determination. Appellants challenged the Examiner's determination that "it would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama **because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor**". Appellants challenged the Examiner to cite art for his above determination. Since, according to the Examiner, "the feature is very well known in any type of computer architecture field", it should have been very easy for the Examiner to cite such evidence.

The Examiner now cites "Shimoda (5,210,861), fig. 1, as showing the use of having data from a local cache 3A instead of having data from a common memory 7c every time to increase processing speed. Appellants respectfully respond that Shimoda does not teach or suggest, "the use of having data from a local cache 3A instead of having data from a common memory 7c every time to increase processing speed", as argued by the Examiner. Appellants respectfully requested the Examiner to cite the column and line number for such teaching should he maintain this argument – he failed to do so.

Morris Mano, page 502, lines 13-14 is relied upon by the Examiner as teaching the use of a cache to increase speed processing of a processor.

As for Morris, Appellants' response is that Morris teaches:

> The fundamental idea of cache organization is that by keeping the most the most frequently accessed instructions and data in the fast cache memory, the average memory access time will approach the access time of the cache. Although the cache is only **a small fraction of the size of main memory**, a large fraction of memory requests will be found in the fast cache memory because of the locality of reference property of programs (page 502, lines 15-20).

But Morris Mano further discloses:

> Such a fast small memory is referred to as a cache memory. It is placed **between the CPU and MAIN MEMORY** as illustrated in Fig. 12-6 (page 502, lines 10-11).

Accordingly, Shimoda and Morris Mano fail to provide any additional teaching that would have led one of ordinary skill in the art at the time of Appellants' invention that "it would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama **because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor**", as suggested by the Examiner. The Examiner's determination is supposition not supported by fact.

Response to Examiner's rebuttal (12) (Office Action dated June 6, 2002, page 15, line 16 – page 15, line 15). The Examiner admits that Aoyama "does not show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor" (Office Action dated May 15, 2001, page 5, lines 1-4). The Examiner relies upon Asano as "teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory" (Office Action dated May 15, 2001, page 5, lines 4-7).

Appellants respectfully traverse the Examiner's interpretation of Asano and point out that Asano's processor DMM1-DMMk (11a-11k) are ALL digital signal processors (Figs. 1 & 2; Col. 9, lines 46-53) which are used exclusively for video signal processing (col. 5, lines 50-55; col. 6. lines 57- col. 8. Line 21). Accordingly, since each unit processor DMM1-DMMk is in charge of processing image signals for a plurality of sectional frames which are not contiguous but separated from each other, and all the unit processor simultaneously

begin processing in synchronism with the state of a new picture frame, each of processors DMM1-DMMk appear to perform "vector" processing, and not "scalar" processing. Accordingly, it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Asano similarly fails to teach or suggest a "synchronizing circuit for coupling said core of said first processor to said core of said second processor", as required by Claims 6 and 36. Appellants respectfully requested the Examiner to identify the above circuit in Asano – he did not do so. This is yet another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Asano further fails to teach or suggest, "one and only one common memory coupling the local memory of the first processor to the local memory of the second processor", as required by Claim 36, since Asano clearly discloses "multiple" common memories 10a-10n coupling processors DMM1-DMMk (Figs. 1 & 2). This is yet still another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Further, while Asano may well disclose a synchronizing circuit, it is for the processors to "access a common memory" (e.g., fig. 6, el. 71 controlling the plurality processors to access a common memory 62; and col. 12, lines 58-61) – NOT for coupling the core of the first processor to the core of the second processor.

Appellants traverse the Examiner's determination that "it does not matter whether Asano teaches or does not teaches a synchronizing circuit for coupling the core of said first processor to the core of said second process because Aoyama teaches the feature as stated in the rejection above" (Office Action dated June 6, 2002, page 16, lines 8-11). Appellants respond that it certainly does matter! It goes to the core of whether or not one of ordinary skill in the art at the time of the invention would have been motivated to combine the two teachings.

Applicants further disagree with the Examiner's position that Appellants cannot attack the references individually (Office Action dated June 6, 2002, page 15, line 19 – page 16, line 3). Appellants cautioned the Examiner not to presume that his combination of Asano and Aoyama is THE PRIOR ART. Appellants respectfully point out that they are entitled to analyze the references individually first, and then in combination to determine what is the prior art. In Graham v. John Deere Co., 148 USPQ 459 (U.S. Sup. Ct. 1966), the U.S. Supreme Court clearly and explicitly compared Scoggin's invention first to the Lohse patent individually, thereafter to the Mellon patent individually, and thereafter to the Livingstone patent individually. 148 USPQ 459, 472. Such an individual assessment of the prior art references is considered well-settled law in view of the fact that the obviousness statute, 35 USC 103, "refers to the difference between the subject matter sought to be patented and the prior art, meaning what was known before as described in section 102". Graham, 148 USPQ 459, 465-466 (quoting the Senate and House Reports, S. Rep. No. 1979, 82nd Cong., 2d Sess. (1952); H.R. Rep. No. 1923, 82d Cong., 2d Sess. (1952)). Thus, Graham requires that each reference be assessed individually to ascertain how it differs from the claims. This should be clear by realizing that 35 USC 103 has as its predicate 35 USC 102. If the factual inquiry of ascertaining the differences between the prior art and the claims results in a finding that there are no differences between the prior art (e.g., any single reference) and the claims, then a rejection under 35 U.S.C. 102 would be proper without any necessity of a rejection under 35 USC 103. Thus, when ascertaining differences between the prior art and the claims, each reference is to be taken individually as under 35 USC 102.

Further, Appellants' arguments do in fact consider the effect of combining the references. In re Sernaker, 217 USPQ 1 (Fed. Cir. 1983), states well the test for determining whether the ascertained differences between the prior art and the claims are such that the claimed subject matter as a whole would have been obvious: "whether a combination of the teachings of all or any of the references would have suggested (expressly or by implication) the possibility of achieving further improvement by combining such teachings along the line of the invention". Thus, the teachings of the prior art are to be evaluated as a combined whole, but after the differences between the prior art and the claims have been ascertained. Both In re Keller, 208 USPQ2d 871, 880-881, and In re Merck & Co., 800 F.2c 1091, 231 USPQ 375 (Fed. Cir. 1986), relied on by the Examiner, assess the combined teachings of the prior art only after the differences between the prior art and claims had been determined.

Response to Examiner's rebuttal (13) (Office Action dated December 6, 2002, page 16, line 19 – page 17, line 10). Appellants respectfully traverse the Examiner's determination that "Asano clearly discloses one and only one common memory coupling the local memory of the first processor to the local memory of the second processor". In reality, while Asano discloses in Fig. 6 a common memory 62 peripherally connected to DSPs 63a, 63b ... 63n. Appellants fail to see where common memory 62 "couples" the local memory of any one of DSPs 63a, 63b ... 63n to another one of the DSPs – the DSPs are already coupled to each other. Nothing in the Examiner's reference to Figure 1 or Figure 6 does anything to counter Appellants' contention that Asano's DSP are already coupled to each other – memory 62 DOES NOT couple one DSP to another. The Examiner's determination is supposition not supported by fact.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to

combine the relevant teachings of the references", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest ALL the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The Examiner has not satisfied the above requirements in rejecting Claims 6 and 36.

Claims 7, 9, 10-15 and 17 stand allowable as depending from allowable claims and include further limitation not taught or suggested by the references of record.

Claim 7 further defines the apparatus of Claim 6, wherein said second processor is the main processor of said apparatus. The Aoyama reference does not teach or suggest a "main processor" with processors DMM1-DMMk. As a result, Aoyama fails to teach or suggest this further limitation in combination with the requirements of Claim 6. Moreover, since Asano fails to teach or suggest the use of a "main" processor with processors DMM1-DMMk, it fails to overcome the previously identified deficiency of the Aoyama reference.

Response to Examiner's rebuttal (14) (Office Action dated June 6, 2002, page 17, lines 11-18). Appellant respectfully traverse the Examiner's determination that "Aoyama teaches or suggests wherein the second processor is the main processor of the apparatus". The Examiner cites col. 4, line 63, of Aoyama for support. In reality, col. 4, line 63 discloses a "vector processing system". In contrast to the Examiner assertion, Aoyama does not disclose the "vector processing system" is a "main processor".

Claim 9 further defines the apparatus of Claim 7, wherein said second processor is a digital signal processor "DSP". The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 7.

Response to Examiner's rebuttal (15) (Office Action dated June 6, 2002, page 17, lines 19-20). Appellants reaffirm the above argument in support of the allowability of Claim 9.

Claim 10 further defines the apparatus of Claim 6, wherein said program memory of said first processor is ROM memory. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 11 further defines the apparatus of Claim 6, wherein said local memory of said first processor is RAM memory. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 12 further defines the apparatus of Claim 6, wherein said program memory of said second processor is ROM memory. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 13 further defines the apparatus of Claim 6, wherein said local memory of said second processor is RAM memory. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Response to Examiner's rebuttal (16) (Office Action dated June 6, 2002, page 18, lines 5-21). The Examiner is relying upon his own experience and motivation for citing the obviousness of the above additional limitations. The Examiner should cite prior art to support his position. Accordingly, Appellants reaffirm above arguments in support of Claims 10-13.

Claim 14 further defines the apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is physically separate from said first and second processors. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Response to Examiner's rebuttal (17) (Office Action dated June 6, 2002, page 19, line 1 – page 20 line 2). Appellants respectfully submit that the Examiner is improperly relying upon hindsight reconstruction in his conclusions on page 19, line 16 – page 20, line 2. The motivation for the Examiner's combination comes from the Examiner – NOT from the prior art. Accordingly, Appellants reaffirm above the argument in support of claim 14.

Claim 15 further defines the apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is a DPRAM memory. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Response to Examiner's rebuttal (18) (Office Action dated June 6, 2002, page 20, line 3 – page 21, line 4). Appellants reaffirm the above argument in support of Claim 15. Additionally, Aoyama (col. 10, line 13-16 and Fig. 5) specifically describes "multiple" common memories 108(1), 108(2), 108(3) – NOT "a" common memory as required by the present invention. Appellants respectfully submit that the Examiner is improperly relying upon hindsight reconstruction in his conclusions on page 20, lines 17–21. The motivation for the Examiner's combination comes from the Examiner – NOT from the prior art.

Claim 17 further defines the apparatus of Claim 6, wherein said synchronizing circuit ensures that only one of said first and processors utilizes said memory circuit for coupling said local memory of said first processor to said local memory of said second processor, at any one time. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Response to Examiner's rebuttal (19) (Office Action dated June 6, 2002, page 21, lines 6 – page 22, line 12). Appellants reaffirm the above argument in support of Claim 17. Moreover, while the present invention discloses "a synchronizing circuit". Further, Appellants have reviewed the support cited by the Examiner in Aoyama (e.g., col. 5, line 63 and et seq.), and cannot find any support for the Examiner's determination. Appellants respectfully submit that the Examiner is improperly relying upon hindsight reconstruction in his conclusions on page 21, line 21 – page 22, line 6. The motivation for the Examiner's combination comes from the Examiner – NOT from the prior art.

3) Claims 8 and 35 are patentable under 35 U.S.C. 103(a) over Aoyama et. al., in view of Asano et al., further in view of Morris Mano, as set forth below.

Claim 8 further defines the apparatus of Claim 7, wherein said first processor is a microprocessor. Claim 35 further defines the apparatus of Claim 6, wherein said vector processing includes signal processing tasks generally carried out by a DSP and a matrix computation which requires a more powerful structure than that of the DSP and which is generally of the array processor type.

The Examiner admits that Aoyama does not show the scalar processor as a microprocessor (Office Action dated June 6, 2002, page 6, lines 18-19). Asano fails to teach or suggest a "scalar processor" or "a scalar processor that is a microprocessor". While Appellants agree with the Examiner that Mano discusses providing a processor into a microprocessor, it fails to teach or suggest the previously discussed deficiencies of the Aoyama and Asano references as applied to Claims 6 and 7. Accordingly, the 35 U.S.C. 103 rejection is overcome.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this

burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest ALL the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The Examiner has not satisfied the above requirements in rejecting Claims 8 and 35.

4) Claims 34-35 and 37-39 are patentable under 35 U.S.C. 103(a) as being unpatentable over Aoyama et. al., in view of Asano et al., further in view of Applicants' admitted prior art, as set forth below.

Claim 34 further defines the apparatus of Claim 6, wherein said scalar processing encompasses a high-level task which is the monitoring of an application or the management of functioning and tasks which are generally carried out by hard-wired logic which are the protocol processing. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. While Asano does disclose the use of DSPs to perform signal processing on video signals, it fails to teach or suggest the previously discussed deficiencies of the Aoyama and Asano references. It further fails to teach or suggest, "the use of scalar processing encompassed in a high level task which is the monitoring of an application or the management or functioning and tasks generally carried

out by a DSP and the use of array processor type". Moreover Appellants admitted prior art does nothing to overcome the above-identified deficiencies of the Aoyama and Asano references, nor is there in teaching that suggests any combination of the admitted prior art with the teaching of Aoyama and Asano. Accordingly, the 35 U.S.C. 103 rejection of Claim 34 is overcome.

Claim 35 further defines the apparatus of Claim 6, wherein said vector processing includes signal processing tasks generally carried out by a DSP and a matrix computation which requires a more powerful structure than that of the DSP and which is generally of the array processor type. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. While Asano does disclose the use of DSPs to perform signal processing on video signals, it fails to teach or suggest the previously discussed deficiencies of the Aoyama and Asano references. It further fails to teach or suggest, "the use of scalar processing encompassed in a high level task which is the monitoring of a n application or the management or functioning and tasks generally carried out by a DSP and the use of array processor type". Moreover Appellants admitted prior art does nothing to overcome the above-identified deficiencies of the Aoyama and Asano references, nor is there in teaching that suggests any combination of the admitted prior art with the teaching of Aoyama and Asano. Accordingly, the 35 U.S.C. 103 rejection of Claim 35 is overcome.

Independent Claim 37 requires and positively recites, "a main processor comprising a core, **a program memory and a local memory**", "a protocol processor, **of a design other than said main processor**, comprising a core**, a program memory and a local memory**", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

Independent Claim 38 requires and positively recites, "a **main processor** comprising a core, a program memory and a local memory", "a protocol processor comprising a core, a program memory and a local memory, said protocol processor **being of a design which**

enables said protocol processor to execute tasks to which the main processor is not suited", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "a common memory coupling said local memory of said main processor to said local memory of said protocol processor".

Independent Claim 39 requires and positively recites, "a main processor comprising a core, a program memory and a local memory", "a protocol processor comprising a core, **a program memory and a local memory**, said protocol processor **being of a design which enables said protocol processor to execute tasks to which the main processor is not suited"**, "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

The Examiner admits that Aoyama "does not show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor" (Office Action dated June 6, 2002, page 9, line 21 – page 10, line 2). The Examiner relies upon Asano as "teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory" (Office Action dated June 6, 2002, page 10, lines 2-6).

Appellants respectfully traverse the Examiner's interpretation of Asano and point out that Asano's processor DMM1-DMMk (11a-11k) are ALL digital signal processors (Figs. 1 & 2; Col. 9, lines 46-53) which are used exclusively for video signal processing (col. 5, lines 50-55; col. 6. lines 57- col. 8. Line 21). Accordingly, since each unit processor DMM1-DMMk is in charge of processing image signals for a plurality of sectional frames which are not contiguous but separated from each other, and all the unit processor simultaneously begin processing in synchronism with the state of a new picture frame, each of processors DMM1-DMMk appear to perform "vector" processing, and not "scalar" processing. Accordingly, it would not have been obvious to one having ordinary skill in the art at the

time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Asano similarly fails to teach or suggest a "synchronizing circuit for coupling said core of said first processor to said core of said second processor", as required by Claims 6 and 36. Appellants asked the Examiner to identify any such circuit in Asano – he failed to do so. This is yet another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Appellants further point out that the Examiner admits that Aoyama and Asano "do not show the use of the first processor being a protocol processor", (Office Action dated June 6, 2002, page 10, lines 13-14). The Examiner relies upon Appellants' specification page 1, line 6 - page 2, line 11 for teaching that both the concept and advantages of providing protocol processor for performing protocol processing are well known and expected in the art.

Appellants respectfully disagree with the Examiner interpretation of page 1, line 6 - page 2, line 11 of the instant specification. While "protocol processing" may itself be known in the art, there is no teaching or suggestion in Appellants' prior art that it could be combined with the teaching of Aoyama and Asano to obviate the present invention. Appellants further submit that the teaching of page 1, line 6 - page 2, line 11 of the instant specification does not overcome the previously identified deficiencies of the Aoyama and Asano references. Moreover Appellants admitted prior art does nothing to overcome the above-identified deficiencies of the Aoyama and Asano references, nor is there in teaching that suggests any combination of the admitted prior art with the teaching of Aoyama and Asano.

Asano further fails to teach or suggest, "one and only one common memory coupling the local memory of the first processor to the local memory of the second processor", as required by Claim 37 & 39, since Asano clearly discloses "multiple" common memories 10a-10n coupling processors DMM1-DMMk (Figs. 1 & 2). This is yet still another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing, in combination with the teaching of page 1, line 6 - page 2, line 11 of the instant specification. Accordingly, the 35 U.S.C. 103 rejection of Claims 37-39 over a combination of Aoyama, Asano and Appellants' prior art is overcome.

Response to Examiner's rebuttal (20) (Office Action dated June 6, 2002, page 22, line 13 – page 23, line 9). While the Examiner has put forth his OWN theory that, "it would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation power and functionality", the Examiner has provided no evidence to support his determination.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in

the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest ALL the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The Examiner has not satisfied the above requirements in rejecting Claims 34, 35 and 37-39.

5) Claims 34 and 37-39 stand patentable under 35 U.S.C. 103(a) over Aoyama et. al., in view of Asano et al., further in view of Finch, as set forth below.

Claim 34 further defines the apparatus of Claim 6, wherein said scalar processing encompasses a high-level task which is the monitoring of an application or the management of functioning and tasks which are generally carried out by hard-wired logic which are the protocol processing. The Examiner admits that Aoyama fails to teach "the use of scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and tasks which are generally carry out by hard-wired logic which are the protocol processing (Office Action dated June 6, 2002, page 11, lines 5-8). As a result, the Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. While Asano does disclose the use of DSPs to perform signal processing on video signals, it fails to teach or suggest the previously discussed deficiencies of the Aoyama and Asano references. It further fails to teach or suggest, "the use of scalar processing encompassed in a high level task which is the monitoring of an application or the management or functioning and tasks generally carried out by a DSP and the use of array processor type". Even if, arguendo, Finch discloses "a protocol processor performing protocol processing", Appellants' response is "so what"? Finch does not overcome the previously discussed deficiencies of Aoyama and Asano and there is no teaching or suggestion in Finch suggesting that it could be combined with the teachings of

Aoyama and Asano in the manner suggested by the Examiner. Accordingly, the 35 U.S.C. 103 rejection of Claim 34 is overcome.

Independent Claim 37 requires and positively recites, "a main processor comprising a core, **a program memory and a local memory**", "a protocol processor, **of a design other than said main processor**, comprising a core**, a program memory and a local memory**", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

Independent Claim 38 requires and positively recites, "a **main processor** comprising a core, **a program memory and a local memory**", "a protocol processor comprising a core, a program memory and a local memory, said protocol processor **being of a design which enables said protocol processor to execute tasks to which the main processor is not suited**", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "a common memory coupling said local memory of said main processor to said local memory of said protocol processor".

Independent Claim 39 requires and positively recites, "a main processor comprising a core, **a program memory and a local memory**", "a protocol processor comprising a core, a **program memory and a local memory**, said protocol processor **being of a design which enables said protocol processor to execute tasks to which the main processor is not suited"**, "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

The Examiner admits that Aoyama "does not show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor" (Office Action dated June 6, 2002, page 12, lines 5-9). The Examiner relies upon Asano as "teaching the concept and

advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory" (Office Action dated June 6, 2002, page 12, lines 9-13).

Appellants respectfully traverse the Examiner's interpretation of Asano and point out that Asano's processor DMM1-DMMk (11a-11k) are ALL digital signal processors (Figs. 1 & 2; Col. 9, lines 46-53) which are used exclusively for video signal processing (col. 5, lines 50-55; col. 6. lines 57- col. 8. Line 21). Accordingly, since each unit processor DMM1-DMMk is in charge of processing image signals for a plurality of sectional frames which are not contiguous but separated from each other, and all the unit processor simultaneously begin processing in synchronism with the state of a new picture frame, each of processors DMM1-DMMk appear to perform "vector" processing, and not "scalar" processing. Accordingly, it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Asano similarly fails to teach or suggest a "synchronizing circuit for coupling said core of said first processor to said core of said second processor", as required by Claims 6 and 36. If the Examiner can identify such circuit, Appellants respectfully request him to do so. This is yet another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Appellants further point out that the Examiner admits that Aoyama and Asano "do not show the use of the first processor being a protocol processor", (Office Action dated June 6, 2002, page 12, lines 19-20). The Examiner relies upon Finch (col. 8, line 42 and et seq.) for teaching that both the concept and advantages of providing protocol processor for performing protocol processing are well known and expected in the art.

Appellants respectfully disagree with the Examiner interpretation of page 1, line 6 - page 2, line 11 of the instant specification. While "protocol processing" may itself be known in the art, there is no teaching or suggestion in Appellants' prior art that it could be combined with the teaching of Aoyama and Asano to obviate the present invention. Appellants fail to understand how adding the teaching of page 1, line 6 - page 2, line 11 of the instant specification overcomes the previously identified deficiencies of the Aoyama and Asano references.

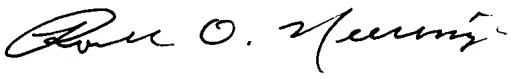
Asano further fails to teach or suggest, "one and only one common memory coupling the local memory of the first processor to the local memory of the second processor", as required by Claim 37 & 39, since Asano clearly discloses "multiple" common memories 10a-10n coupling processors DMM1-DMMk (Figs. 1 & 2). This is yet still another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing, in combination with the teaching of page 1, line 6 - page 2, line 11 of the instant specification. Accordingly, the 35 U.S.C. 103 rejection of Claims 37-39 over a combination of Aoyama, Asano and Finch is overcome.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest ALL the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The Examiner has not satisfied the above requirements in rejecting Claims 34 and 37-39.

For the above reasons, favorable consideration of the appeal of the Final Rejection in the above-referenced application, and its reversal, are respectfully requested.

Respectfully submitted,



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APPENDIX

CLAIMS ON APPEAL:

6. An apparatus, comprising:

a first processor for performing scalar processing, said first processor comprising a core, a program memory and a local memory;

a second processor for performing vector processing, said second processor comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said core of said first processor to said core of said second processor; and

a memory circuit for coupling said local memory of said first processor to said local memory of said second processor.

7. The apparatus of Claim 6, wherein said second processor is the main processor of said apparatus.

8. The apparatus of Claim 7, wherein said first processor is a microprocessor.

9. The apparatus of Claim 7, wherein said second processor is a digital signal processor "DSP".

10. The apparatus of Claim 6, wherein said program memory of said first processor is ROM memory.

11. The apparatus of Claim 6, wherein said local memory of said first processor is RAM memory.

12. The apparatus of Claim 6, wherein said program memory of said second processor is ROM memory.

13. The apparatus of Claim 6, wherein said local memory of said second processor is RAM memory.

14. The apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is physically separate from said first and second processors.

15. The apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is a DPRAM memory.

17. The apparatus of Claim 6, wherein said synchronizing circuit ensures that only one of said first and processors utilizes said memory circuit for coupling said local memory of said first processor to said local memory of said second processor, at any one time. The Asano reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

34. The apparatus of Claim 6, wherein said scalar processing encompasses a high-level task which is the monitoring of an application or the management of functioning and tasks which are generally carried out by hard-wired logic which are the protocol processing.

35. The apparatus of Claim 6, wherein said vector processing includes signal processing tasks generally carried out by a DSP and matrix computation which requires a more powerful structure than that of the DSP and which is generally of the array processor type.

36. (amended) An apparatus, comprising:

a first processor comprising a core, a program memory and a local memory;

a second processor, of a design other than said first processor, comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said first processor to said second processor; and

one and only one common memory coupling said first processor to said second processor.

37. (amended) An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor, of a design other than said main processor, comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor.

38. (amended) An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor comprising a core, a program memory and a local memory, said protocol processor being of a design which enables said protocol processor to execute tasks to which the main processor is not suited;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

a common memory coupling said local memory of said main processor to said local memory of said protocol processor.

39. (amended) An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor comprising a core, a program memory and a local memory, said protocol processor being of a design which enables said protocol processor to execute tasks to which the main processor is not suited;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor.